APPLICATION

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TITLE: **METHOD FOR MANUFACTURING SEMICONDUCTOR DEVICE**

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METHOD FOR MANUFACTURING SEMICONDUCTOR DEVICE

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a method for manufacturing a crystalline silicon thin film, and further to a method for manufacturing a semiconductor device using this crystalline silicon thin film.

2. Description of the Related Art

Conventionally, various techniques are known in this field. That is, an amorphous silicon film formed on a glass substrate, or a quartz substrate is crystallized to fabricate a crystalline silicon film, and then, a thin-film transistor is configured by using this crystalline silicon film.

As for a method for forming a crystalline silicon film, typically two manufacturing methods have been proposed. That is, laser light is irradiated to an amorphous silicon film formed by a plasma CVD method and the like so as to convert this amorphous silicon film into a crystalline silicon film. A heating process is carried out to an amorphous silicon film formed by a plasma CVD method and the like, so that this amorphous silicon film is converted into a crystalline silicon film.

As to such a crystalline silicon film forming method, one technique is known from Japanese Laid-open Patent Application No. 6-232059. This technique is used to crystallize the amorphous silicon film under lower temperatures by using the metal elements that accelerates the crystallization of silicon.

The present applicant recognized by their research that when a metal element that accelerates the crystallization of silicon is used to

obtain the crystalline silicon film, and further the thin-film transistor is manufactured by using this crystalline silicon film, the dispersion of characteristics of this thin-film transistor tends to occur.

SUMMARY OF THE INVENTION

In the above circumstances, an object of the present invention is to provide a technique for forming a crystalline silicon film by using a metal element that accelerates the crystallization of silicon to prevent the metal element from locally concentrate in this crystalline silicon film.

As a result of extensive study to solve the above problem that the concentration of metal element occurs in the crystalline silicon film, the present applicant could recognize the below-mentioned items.

Fig. 2 represents an observation result of a lump of a nickel element in a crystalline silicon film of 1 μm square, which is crystallized by using the nickel element.

A description will now be made of a method for manufacturing the crystalline silicon film from which data indicated in Fig. 2 could be obtained. First, an amorphous silicon film having a thickness of 500 Å is formed on a glass substrate by a plasma CVD method. Then, a nickel acetate solution is coated on the surface of this amorphous silicon film. Under this state, it is realized that the nickel element is made in contact with the surface of the amorphous silicon film. The heating process is carried out for 4 hours at a heating temperature (indicated as SPC temperature in the figure) described in Fig. 2. As a result, a crystalline silicon film formed on the glass substrate can be obtained.

The differences between the samples to obtain three sorts of data

shown in Fig. 2 are the heating temperatures to obtain the crystalline silicon film.

The method for observing the lump of nickel element indicated in Fig. 2 is performed in accordance with the following manner. That is, the obtained crystalline silicon film is etched away by FPM (mixture solution of fluorine compound and hydrogen peroxide) to remove the region where nickel is lumped (this region is nickel silicide). Then, the total number of removed holes is counted by using an electron microscope.

In Fig. 3, there are shown conditions of holes indicative of this region where nickel is lumped. That is, Fig. 3 is a photograph showing the state after the surface of the crystalline silicon film has been etched away by FRM, taken by an electron microscope.

Although this observation method could not measure the absolute value of the number of the lumps of nickel element, this observation method could evaluate the relative number.

As indicated in Fig. 2, the higher the temperature of the heating process is increased, the smaller the number of lumps of the detected nickel elements become. However, when the number of the lumps of nickel element is measured by SIMS (secondary ion mass spectroscopy), the concentrations of the nickel elements are substantially equal to each other, irrelevant to the differences in the temperatures at the heating process (during SPC). As a consequence, it is assumed that as to segregation of the nickel element, the higher the temperature at the heating process is increased, the larger each of these lumps becomes.

Also, it is recognized that the higher the temperature at the heating process is increased, the longer the diffusion distance of the nickel

element becomes. This diffusion distance "D" may be expressed by approximately $D_0\, t \exp(-\Delta E/kT)$. In this formula, symbol "D_0" indicates a properly selected constant, symbol "t" denotes a heating time, symbol "ΔE" denotes a properly selected constant, symbol "K" is Boltzmann constant, and symbol "T" represents the heating temperature (SPC temperature). The trend expressed by this formula may be applied not only to the nickel element, but also to other metal elements.

As apparent from the above-described formula, if the heating temperature is increased, then the diffusion distance of the nickel element is increased in the exponential function manner. On the other hand, the higher the heating temperature is increased, the larger the lumps of the nickel element becomes.

Also, as a result of the research made by the Applicant, it could be recognized that the nickel element can be easily concentrated into the region where the stress distortion is concentrated.

The present invention has been accomplished based upon the above-described recognitions, as disclosed in the following descriptions.

According to one aspect of the present invention, a method for manufacturing a semiconductor device is characterized by comprising the steps of:

forming an amorphous silicon film on a substrate having an insulating surface;

patterning said amorphous silicon film to form a predetermined pattern;

holding a metal element that accelerates the crystallization of silicon in such a manner that said metal element is brought into contact with said amorphous silicon film;

performing a heating process to crystallize said amorphous silicon film, thereby being converted into a crystalline silicon film; and

etching a peripheral portion of the pattern of said crystalline silicon film.

According to another aspect of the present invention, a method for manufacturing a semiconductor device is characterized by comprising the steps of:

forming a region into which a defect and/or stress is concentrated in a preselected region of an amorphous silicon film;

holding a metal element that accelerates the crystallization of silicon in such a manner that said metal element is brought into contact with said amorphous silicon film;

performing a heating process so as to crystallize said amorphous silicon film; and

etching said preselected region.

According to a further aspect of the present invention, a method for manufacturing a semiconductor device is characterized by comprising the steps of:

forming a region into which a defect and/or stress is concentrated in a preselected region of an amorphous silicon film;

holding a metal element that accelerates the crystallization of silicon in such a manner that said metal element is in contact with said amorphous silicon film;

performing a heating process so as to crystallize said amorphous silicon film and, at the same time, segregating said metal element into said preselected region; and

etching said preselected region.

In each of the above-described manufacturing methods according to the present invention, generally speaking, when a glass substrate is utilized, the temperature of the heating process is preferably selected to be 450°C to 700°C.

When a quartz substrate is used as the substrate, the temperature of the heating process is preferably selected to be 800°C to 1100°C. In particular, since such a high temperature is selected, it is preferable to obtain the high crystallinity.

In accordance with the present invention, examples of metal element that accelerates the crystallization of silicon, one or plural sorts of metal elements selected from Fe, Co, Ni, Ru, Rh, Pd, Os, Ir, Pt, Cu, and Au may be used.

As a method for introducing this metal element, it is preferable to use a solution containing the metal element. Since the metal element can be formed in the film shape according to this method using the solution, there is a merit that this metal element can be held in such a manner that this metal element is uniformly brought into contact with the surface of the amorphous silicon film.

The present invention also possesses such a particular feature that the concentration of the metal element can be easily controlled. In general, the concentration of the metal element that accelerates the crystallization of silicon should be reduced as low as possible. As a consequence, it is a very important technique to control an amount of a metal element to be introduced.

A description will now be made of the method using the metal element solution. First, when Ni is used as the metal element that accelerates the crystallization of silicon, it is possible to use at least one

sort of solution selected from such nickel compounds as nickel bromide. nickel acetate, nickel oxalate, nickel carbonate, nickel chloride. nickel iodide, nickel nitrate, nickel sulfate, nickel formate, nickel acetyl acetate. 4-cyclohexyl butyric nickel, nickel oxide, nickel hydroxide, and 2-ethylhexane nickel.

Also, Ni may be contained in a non-polarity solution selected from at least one of benzene, toluene, xylene, carbon tetrachloride. chloroform, ether, trichloroethylene, and Freon.

In the case that Fe (iron) is used as the metal element that accelerates the crystallization of silicon, various materials known as iron salt may be selected from, for instance, iron (I) bromide ($FeBr_26H_2O$). iron (II) bromide ($FeBr_36H_2O$), ferric acetate ($Fe(C_2H_3O_2)_3xH_2O$). ferrous chloride ($FeCl_24H_2O$), ferric chloride ($FeCl_3$ $6H_2O$), ferric fluoride (FeF_33H_2O), ferric nitrate ($Fe(NO_3)_39H_2O$), ferrous phosphate ($Fe_3PO_48H_2O$), and ferric phosphate ($FePO_4$ $2H_2O$)

In such a case that Co (cobalt) is used as the metal element that accelerates the crystallization of silicon, various materials known as cobalt salt functioning as a cobalt compound may be selected from. for instance, cobalt bromide ($CoBr6H_2O$), cobalt acetate ($CoF_{2x}H_2O$). cobalt chloride ($CoCl_26H_2O$), cobalt fluoride ($CoF_{2x}H_2O$), and cobalt nitrate (Co(No3)26H2O).

When Ru (ruthenium) is used as the metal element that accelerates the crystallization of silicon, various materials known as ruthenium salt functioning as a ruthenium compound may be selected from. for example, ruthenium chloride ($RuCl_3H_2O$).

When Rh (rhodium) is used as the metal element that accelerates

the crystallization of silicon, various materials known as rhodium salt functioning as a rhodium compound, for instance, rhodium chloride ($Rhcl_3 3H_2O$) may be used.

When Pd (palladium) is used as the metal element that accelerates the crystallization of silicon, various materials known as palladium salt functioning as a palladium compound, for instance, palladium chloride ($Pdcl_2 2H_2O$) may be used.

When Os (osmium) is used as the metal element that accelerates the crystallization of silicon, various materials known as osmium salt functioning as a osmium compound, for instance, osmium chloride ($Oscl_3$) may be used.

When Ir (iridium) is used as the metal element that accelerates the crystallization of silicon, various materials known as iridium salt functioning as a iridium compound, for instance, iridium trichloride ($IrCl_3 3H_2O$) and iridium tetrachloride ($IrCl_4$) may be used.

When Pt (platinum) is used as the metal element that accelerates the crystallization of silicon, various materials known as platinum salt functioning as a platinum compound, for instance, platinum (II) chloride ($PtCl_4 5H_2O$) may be used.

When Cu (copper) is used as the metal element that accelerates the crystallization of silicon, various materials as a copper compound, for instance, copper (II) acetate ($Cu(CH_3COO)_2$, copper (II) chloride ($CuCl_2 2H_2O$), and copper (II) nitrate ($Cu(NO_3)_2 3H_2O$) may be used.

When Au (gold) is used as the metal element that accelerates the crystallization of silicon, various materials as a gold compound, for instance, gold trichloride ($AuCl_{3x}H_2O$) and gold chloride salt

($AuHCl_44H_2O$) may be used.

As represented in Fig. 6, for example, a peripheral portion 108 of a pattern 100 of a crystalline silicon film to be obtained is removed. In this region 108, stress distortion and defects, which are formed when the pattern 103 is obtained, are concentrated to a peripheral portion 106. Then, the metal element that accelerates the crystallization of silicon is present with high concentration within this region 106. As a consequence, it is possible to obtain a crystalline silicon film 100 from which the adverse influence caused by this metal element has been eliminated by removing this region 106.

In such a case that a region into which defects and stress are artificially concentrated is formed, a diffusion distance "D" of the metal element will now be considered. Concretely speaking, since another distance "d" defined from a central portion of an eventually obtained pattern to the region into which the defects and the stress are concentrated is selected to be d=D/30 to D, the metal element can be effectively and forcibly moved to such a region into which the above-explained defects and stress are concentrated. More specifically, the above-explained metal element can be removed from the channel forming region of the thin-film transistor, so that such a thin-film transistor operable under stable condition can be manufactured.

As described above, since the region into which the defects and stress are concentrated is used as the gettering region of the metal element that accelerates the crystallization of silicon, the reliability of the semiconductor device using the crystalline silicon film can be improved.

BRIEF DESCRIPTION OF THE DRAWINGS

For a better understanding of the present invention, reference is made of the following detailed description to be read in conjunction with the accompanying drawings, in which:

Figs. 1A-1E schematically show a manufacturing process of a thin-film transistor according to an embodiment of the present invention;

Fig. 2 graphically represents the number of lumps of nickel element contained in a crystalline silicon film per unit area;

Fig. 3 is a photograph for showing the crystalline silicon film;

Figs. 4A-4E schematically indicate a manufacturing step of a thin-film transistor according to another embodiment of the present invention;

Figs. 5A-5D schematically indicates a manufacturing step of a thin-film transistor according to another embodiment of the present invention;

Fig. 6 is a top view for representing a patterning condition of the crystalline silicon film;

Fig. 7 is a top view for indicating a patterning condition of a crystalline silicon film manufactured by the present invention;

Figs. 8A-8D schematically indicate a manufacturing step of a thin-film transistor according to a further embodiment of the present invention; and

Figs. 9A-9D schematically indicate a manufacturing step of a thin-film transistor according to a still further embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring now to drawings, various embodiments of the present invention will be described.

[EMBODIMENT 1]

It should be noted that as a metal element that accelerates the crystallization of silicon, the below-mentioned embodiments mainly use nickel. This is because the highest advantages could be achieved in the embodiments when nickel is used. Also, as other preferable metal elements except for nickel, there are palladium, platinum, and copper. When these preferable metal elements are used, a similar effect to that of nickel may be obtained.

Fig. 1 schematically represents a manufacturing step of a thin-film transistor according to an embodiment 1 of the present invention. First, a silicon oxide film 102 having a thickness of 3000 Å is formed as an underlayer film on a glass substrate 101 by either a plasma CVD method or a sputtering method. This silicon oxide film 102 owns such a function to block a diffusion of an impurity from the glass substrate 101. Also, this silicon oxide film 102 has another function to relax the stress produced between the glass substrate 101 and a silicon thin-film which will be formed in a later step.

Next, an amorphous silicon film (not shown) having a thickness of 500 Å is formed on the silicon oxide film 102 by a plasma CVD method. Next, an island-shaped pattern 103 made of an amorphous silicon film is formed by patterning a pattern larger than an active layer of a finally manufactured thin-film transistor (see Fig. 1A).

As for a plasma CVD film having a thickness of 500 Å used in this embodiment 1, a recognition could be made in that the maximum diffusion distance of the nickel element under plasma CVD method of

550°C and 4 hours is approximately 2 μm. As a consequence, a distance "d" shown in Fig. 6 is selected to be 2 μm, and Fig. 6 represents a condition under which the thin-film transistor of Fig. 1 is viewed from the upper surface. It should be noted that a distance indicated by "a" is selected to be 0.5 μm.

It is desirable to form this pattern by a plasma etching process having vertical anisotropy. This is because when a plasma etching treatment is carried out, the stress distortion and defects caused by the plasma damages would be readily produced in the edge regions of the island-shaped pattern.

Then, a nickel acetate solution whose concentration has been controlled to a predetermined value is coated by a spin coat method in order that the nickel element 104 is held in contact with an exposed surface of the island-shaped pattern 103 made of the amorphous silicon film (see Fig. 1A).

Under this condition, the heating process at 600°C is performed for 4 hours. The temperature of this heating process is desirably selected to be higher temperatures in the temperature range where the glass substrate 101 can endure the higher temperatures. As a result, when the quartz substrate is used, the heating temperature is preferably selected to be from 800°C to 1100°C for the crystallization purpose.

The island-shaped pattern 103 of the amorphous silicon film is crystallized by performing this heating process. At this time, the nickel element disperses to the peripheral portion of the pattern 103 and concentrates thereto. This concentration to the peripheral portion of the pattern 103 is emphasized in connection with the temperature increase of the heating process.

In accordance with the diffusion of this nickel element, the crystallization of the amorphous silicon film is advanced, so that the pattern 103 is converted into a crystalline silicon film 105.

Also, at this time, the nickel element is concentrated to an edge region of the pattern into which the plasma damage and the stress distortion are concentrated (see Fig. 1B).

Next, an exposed region of 108 is removed by an etching process by using a resist mask 107. In other words, the region into which the nickel element is concentrated is removed by a etching treatment. An active layer 100 of a thin-film transistor is accomplished by this etching step (see Fig. 1C).

Now, as shown in Fig. 6, in the region of 108 to be removed, a dimension indicated as "a" is selected to be 20 μm. In this embodiment, a dimension indicated by "d" is selected to be 20 μm, and then a rectangular pattern defined by 15 μm to 30 μm is obtained as indicated in this drawing. This rectangular pattern 100 becomes an active layer for constituting the thin-film transistor.

Since the region 106 into which the nickel element has been concentrated is present in the region 108 to be removed in the structure of this embodiment, such a condition can be eventually realized under which substantially no lump of the nickel element is present in the active layer indicated by 100.

Furthermore, an aluminum film containing scandium at 0.2 wt% is formed by a sputtering method or an electron beam vapor deposition method. The reason why scandium is contained in the aluminum film is to suppress an occurrence of "hillock" (prickle-shaped projection, or needle-shaped projection) caused by the unusual growth of aluminum in

the succeeding step.

Then, this aluminum film is patterned to thereby form a gate electrode 111. Next, the anode oxidation is carried out in the electrolytic solution by using the gate electrode 111 as the anode, so that an anode oxide film 112 is formed. A thickness of this anode oxide film 112 is selected to be 500 Å. The formation of this anode oxide film 112 can provide such a great advantage that the occurrence of "hillock" is suppressed. Also, when the thickness of this anode oxide film 112 is made thick, an offset gate region may be formed in a succeeding step to implant an impurity ion (see Fig. 1D).

When the semiconductor under condition of Fig. 1D is obtained, a P (phosphorus) ion is implanted by a plasma doping method. In this manufacturing step, the gate electrode 111 may constitute the mask, so that a source region 113, a channel forming region 114, and a drain region 115 are formed in the self-alignment manner (see Fig. 1D).

In this example, the N-channel type thin-film transistor is manufactured by an implantation of P ion. However, when a B ion is implanted, a P-channel type thin-film transistor may be alternatively manufactured.

Next, a silicon oxide film 116 is formed as an interlayer insulating film with a thickness of 7000 Å by a plasma CVD method. Furthermore, a contact hole is formed, and both a source electrode 117 and a drain electrode 118 are formed by a stacked layer film of a titanium film, an aluminum film, and a titanium film. In this manner, a thin-film transistor as shown in Fig. 1E may be accomplished.

When the above-described manufacturing steps of this embodiment 1 are used, it is possible to suppress such a fact that the region to which

the nickel element is concentrated is formed in the active layer 100. As a consequence, the difficulties caused by the presence of the nickel element can be avoided.

[EMBODIMENT 2]

This embodiment 2 is related to an arrangement for obtaining a thin-film transistor having a higher crystallinity than that of the embodiment 1 by combining the manufacturing steps shown in the embodiment 1 with irradiation of laser light.

In Figs. 4A-4E, there is shown a manufacturing step according to this embodiment 2.

Similar to the manufacturing steps indicated in Fig. 1, a silicon oxide film 102 is formed as an underlayer film on a quartz substrate 401. In this embodiment, the silicon oxide film 102 having a thickness of 5000 Å is formed in order to buffer, or relax stress executed between the quartz substrate and a silicon film which will be formed later.

Next, an amorphous silicon film having a thickness of 1000 Å is formed by a low pressure thermal CVD method. Subsequently, this amorphous silicon film is patterned to thereby form an island-like pattern 103 (see Fig. 4A).

Then, a nickel acetate solution is coated by a spin coat method, and as indicated by reference numeral 104, the nickel element held under such a condition that this nickel element is brought into contact with the surface of the island-like pattern 103 made of the amorphous silicon film in a film shape (see Fig. 4A).

Thereafter, the heating process is carried out at 850°C for 4 hours, so that the island-like pattern 103 made of the amorphous silicon film is

converted into a crystalline silicon film. In this step, since the heating temperature is high, the nickel element is highly concentrated into the peripheral portion of the pattern (see Fig. 4B).

As a result, a crystalline silicon film 105 and also a region 106 where the nickel element is concentrated can be obtained. Then, the peripheral portion 106 of the pattern is removed by an etching process using the resist mask 107. At this step, such a region where the nickel element is present in the concentrated manner is selectively removed (see Fig. 4C).

Then, a crystalline silicon film 402 having an island-like pattern for constituting an active layer of a thin-film transistor is obtained by removing the resist mask 107. The region indicated by this reference numeral 402 corresponds to a region indicated by reference numeral 109 of Fig. 4B.

Subsequently, as represented in fig. 4D, laser light is irradiated to the resultant semiconductor device. The crystallinity of the crystalline silicon film 402 having the island-like pattern can be improved by a laser irradiation.

Also, in accordance with this embodiment 2, after the laser light irradiation, the heating process is carried out at 800°C for 2 hours. The defects occurred irradiating this laser light in the film can be reduced by this heating process (see Fig. 4E).

It should be understood that such a crystalline silicon film having sufficiently high crystallinity may be obtained, even if this second heating process is not carried out. As a result, when the overall manufacturing state is wanted to be simplified, this second heating step may be omitted.

After the active layer 402 made of the crystalline silicon film has been obtained in this manner, a thin-film transistor using the active layer 402 is fabricated in accordance with the steps described in Embodiment 1.

[EMBODIMENT 3]

This embodiment 3 relates to such a structure that a heating process is carried out instead of the laser light irradiation in the manufacturing steps shown in Fig. 4D. Figs. 5A-5D show manufacturing steps of this embodiment. First, a silicon oxide film 102 having a thickness of 5000 Å is formed as an underlayer film on a quartz substrate 401 by a plasma CVD method. Next, an amorphous silicon film (not shown) having a thickness of 1000 Å is formed by a low pressure thermal CVD method.

Next, this amorphous silicon film is patterned to thereby form an island-like pattern 103 as indicated in Fig. 5A. Furthermore, a nickel acetate solution is coated by a spin coat method, and a nickel element is provided in a film shape as indicated by reference numeral 104 (see Fig. 5A).

Then, a heating process is executed at 850°C for 4 hours, so that a crystalline silicon film 105 is formed. Under this state, the nickel element is concentrated around this crystalline silicon film 105 (see Fig. 5B).

Next, a resist mask 107 is arranged to etch away a region indicated by reference numeral 108 in Fig. 5C. In this case, the region 105 is slightly etched away for a small margin.

As described above, the island-like pattern 102 made of the

crystalline silicon film is obtained, as illustrated in Fig. 5D. It should be noted that this pattern 402 will constitute an active layer of a thin-film transistor in a later step.

According to this embodiment, the heating process is again carried out under such a state as shown in Fig. 5D. thus, the crystallinity of the island-like pattern 110 can be furthermore improved by performing this second heating process. It should be noted that laser light or intense light may be irradiated after this second heating process is performed.

[EMBODIMENT 4]

Referring now to Fig. 7, a manufacturing method of an embodiment 4 will be explained. This embodiment 4 is featured as follows. A plurality of openings are formed in an amorphous silicon film around a region 701 which will finally constitute an active layer of a thin-film transistor. A metal element that accelerates the crystallization of silicon is segregated in the region where the opening is formed.

To execute this embodiment 4, an amorphous silicon film 700 is formed on a substrate having a proper insulating surface by a plasma CVD method, or a low pressure thermal CVD method. Next, a portion of the amorphous silicon film is etched away, as represented by reference numeral 702, so as to form openings. It should be understood that the shape of the openings may not be limited to a rectangular shape, but may be a circular shape or a slit shape.

In this embodiment, nickel is used as the metal element that accelerates the crystallization of silicon. After the above-described opening has been formed, a nickel acetate solution whose concentration

is controlled to a predetermined value is coated, and the nickel element is brought into contact with the amorphous silicon film 700 in a film shape to be held.

Then, the heating process is carried out, so that the amorphous silicon film 700 is crystallized. At this time, the nickel element is concentrated to an opening portion indicated by reference numeral 702. This concentration of nickel elements caused by such a reason that defects and stress distortion are concentrated to the region of the opening 702.

The structure as illustrated in this embodiment 4 may become effective in the case that a diffusion distance of a metal element is long, and further a dimension of a pattern is small. For example, this structure of the embodiment 4 becomes effective when a very fine integrated circuit is constituted by using a quartz substrate.

In Fig. 7, also a distance indicated as "c" must satisfy the following condition:

$$c = D/30 \text{ to } D,$$

$$D = D_0\ t \exp(-\Delta E/kt).$$

It should be understood that, generally speaking, the diffusion distance of the metal element indicated by "D" may be actually measured for the sake of simplicity.

In this condition, symbol "D" is a maximum diffusion distance, whereas a minimum diffusion distance is substantially one out of several tens of this maximum diffusion distance. If the distance indicated by the above symbol "c" is made shorter than this minimum diffusion distance, it is possible to make up an arrangement from which the nickel element is completely removed. Concretely speaking, when

the value of "c" is selected to be shorter than, or equal to 5μm, the nickel concentration can be made very low. The above-explained value of "D" may become greatly different from each other, depending upon the film forming conditions of the starting films, the film forming methods thereof, and further the heating methods thereof. The typical value of "D" is 1μm to 5μm. As a result, the value of "d" is selected to be smaller than, or equal to 2 μm, preferably smaller than, or equal to 1 μm.

[EMBODIMENT 5]

Figs. 8A-8D schematically show manufacturing steps according to an embodiment 5 of the present invention. In this manufacturing step shown in Fig. 8, a quartz substrate is used as a substrate. A silicon oxide film 802 having a thickness of 5000Å is firstly fabricated as an underlayer film on the quartz substrate by a plasma CVD method. Next, an amorphous silicon film (not shown) having a thickness of 7000 A is formed. Then, this amorphous silicon film is patterned to thereby form a pattern as indicated by reference numeral 803 of Fig. 8A.

Subsequently, a nickel acetate solution whose concentration is controlled to a preselected value is coated, and then a nickel element is formed in such a manner that this nickel element is made in a film shape as indicated by reference numeral 803 (see Fig. 8A).

Next, the heating process is performed at 950 °C for 4 hours so as to obtain a crystalline silicon film 804.

Thereafter, a surface of a crystalline silicon film having an island-shape indicated by reference numeral 805 is etched by using the isotropic etching means. In this step, a crystalline silicon film 806

having a thickness of 1500 Å is obtained (see Fig. 8C).

Subsequently, the thermal oxidation is carried out at 850°C, so that a thermal oxidation film having a thickness of 500 Å is formed on an exposed surface of the island-like crystalline silicon film 806. In this manner, an active layer 806 made of the crystalline silicon film is obtained which can be utilized in a thin-film transistor (see Fig. 8D).

[EMBODIMENT 6]

This embodiment 6 is related to such a structure capable of further emphasizing the eliminating effect of the metal element that accelerates the crystallization of silicon. In Figs. 9A-9D, there are shown manufacturing steps according to this embodiment 6. First, a silicon oxide film 902 having a thickness of 3000 Å is formed as an underlayer film on a glass substrate 901.

Next, an amorphous silicon film having a thickness of 500 A is formed by a plasma CVD method. Furthermore, this amorphous silicon film is patterned to thereby form an island-like region indicated by reference numeral 903. Then, a nickel acetate solution whose concentration is controlled to a predetermined value is coated by a spin coat method, and a nickel element is provided in a film shape as indicated by reference numeral 904 (see Fig. 9A).

Subsequently, a resist mask 905 is positioned so as to implant a P (phosphorous) ion. In this manufacturing step, the P ion is implanted into a region denoted by reference numeral 906. Defects are formed in the region denoted by reference numeral 906 in higher density by performing the implantation of P ion. Also, no P ion is implanted into another region denoted by reference numeral 907 (see Fig. 9B).

Next, the resist mask 905 is removed to thereby perform the heating process at 550°C for 4 hours. In this step, the overall amorphous silicon film is crystallized. At this time, the nickel element is concentrated to a region denoted by reference numeral 906 and located at an edge peripheral portion of the pattern, indicated by reference numeral 903. This concentration effect of the nickel element is caused by such a fact that P (phosphorous) having the gettering effect of the metal element is implanted into the region 906, and further, the defects are formed in the region 906 at higher density by an implantation of P ion.

Thereafter, as indicated in Fig. 9C, another resist mask 908 is newly arranged in order to etch away the exposed region of the silicon film. Thus, it is possible to obtain a region 909 made of the island-like crystalline silicon film from which the nickel element has been removed. It should be noted that although the phosphorous ion is used in the above-described manufacturing step, an oxygen ion may be used. Alternatively, it is possible to use ions of inert elements with respect to the semiconductor material, for example, silicon ions or argon ions.

As previously described in detail, according to the present invention, it is possible to form the pattern of the crystalline silicon film having a small portion, or no portion into which the metal element has been concentrated in the following manner. That is, the previously patterned amorphous silicon film is crystallized by a heating process, while using the metal element that accelerates the crystallization of silicon. Furthermore, the peripheral region of the pattern, into which this metal element is concentrated, is removed.

In other words, as to the technique for obtaining the crystalline

silicon film by using the metal element that accelerates the crystallization of silicon, such a novel technique is proposed, which can avoid that the metal element is locally concentrated.

As a consequence, characteristics of thin-film transistors can be improved by utilizing the techniques as disclosed in this specification. Also, the manufacturing yield of the obtained thin-film transistor can be increased. Moreover, the characteristics of the obtained thin-film transistor can be made stable.